VLSI LOGIC CIRCUIT USING
SINGLE ELECTRON TRANSISTOR--- SET

Abstract:

Today's world is in a constant state of growth. VLSI technology is no exception to the above statement. Evolution of electronics, after seeing many phases is now in the research area of single electronics. Single electron transistor (SET) is a device of the above kind. It enjoys advantages of nanometer-scale devices. But it has many constraints as far as in the action of implementation. In this paper, we discuss on the constrains and propose a fault-tolerant architecture for an efficient and robust design of system using SET. We have also design digital logic circuits like AND, OR, NAND using NOR implementation of SET. We have also designed the digital circuits like HALF ADDER, HALF SUBTRACTOR, MUX, DEMUX(2:1) with NOR implementation of SET. The design significantly improves the immunity to permanent and transient faults occurring at transistor level

Key Words: *Evolution, VLSI Technology, Nanometer, Logic Circuits.*

Conclusion: In this paper, various circuit and system level design challenges for SET discussed. This paper also concentrates on the functions robustness and emphasizes the fault tolerance architecture design The proposed circuit architecture, based on redundant layers arranged in a feed-forward manner, is capable of absorbing the effects of multiple simultaneous device failures and still offering a high probability of correct operation.

This approach is fundamentally different from the conventional logic redundancy strategies that rely on multiple identical units and majority decisions on their outputs. It is demonstrated that the proposed design technique offers significantly improved immunity to permanent and transient faults occurring at the transistor level that the design technique presented in this paper can be adopted to a wide variety of cases to address the potential reliability limitations of SET.

INTRODUCTION......

VLSI stands for "Very Large Scale Integration". This is the field which involves packing more and more logic devices into smaller and smaller areas. Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device.

Advantages:
• Speed
• Size
• Number of applications
• Continuous integration of electronic devices.
• Progression of IC towards next technology called VLSI

The Phenomenal advancement of digital integrated circuits and VLSI over the last few decades was made possible mainly by a unique combination of factors, namely:

1) The availability of reliable, mass-producible basic building blocks, i.e., MOS transistors
2) the capability of the manufacturing technologies to reduce the device dimensions and thereby increase the integration density on a continuous basis
3) widespread use of well-defined levels of abstraction that enabled circuit and system designers to develop very complex integrated systems in a hierarchical manner; and
4) the availability of design tools that allowed the designers to increase their productivity in step with the increasing complexity of the systems.

What is a SET?

The single electron transistor or SET is type of switching device that uses controlled electron tunneling to amplify current. A SET is made from two tunnel junctions that share a common electrode. A tunnel junction consists of two pieces of metal separated by a very thin (~1 nm) insulator. The only way for electrons in one of the metal electrodes to travel to the other electrode is to tunnel through the insulator. Since tunneling is a discrete process, the electric charge that flows through the tunnel junction flows in multiples of e, the charge of a single electron
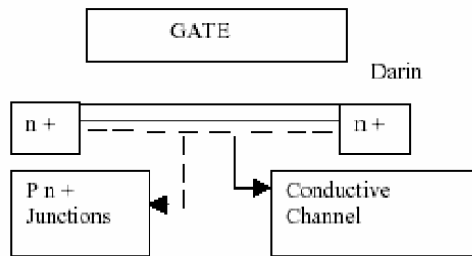
SINGLE ELECTRON TRANSISTOR (SET):

Aggressive scaling of MOSFET dimensions to near-10-nanometer scale is expected to produce a number of fundamental reliability issues related to irregular do pant distributions , parameter fluctuations, and continuity of the channel region. These issues will need to be addressed from the design point of view in order to ensure the feasibility of classical CMOS architectures built with nanometer-scale technologies. In parallel to the scaling of conventional CMOS devices, a wide range of nano- scale quantum device architectures and related technologies are being developed for future nano-scale computation. Single electron transistors (SETS) could be among the most interesting and promising candidates for future nano-electronics because of their particular functionality and complementary characteristics with respect to CMOS. Some preliminary results demonstrated in recent years have also shown the prospect of using silicon-bases fabrication technologies for the integration of SETS with CMOS devices. While a number of successful SET logic applications have been reported by mimicking CMOS functionality, reliability-related questions such as background charge sensitivity and room temperature operation still remain among major issues to be solved for single electronics.
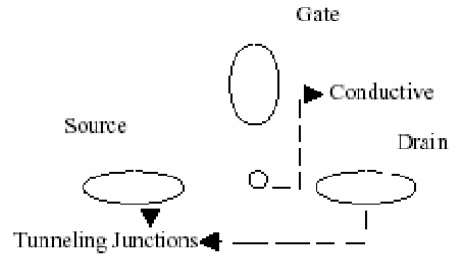
BASIC SYMBOLIC REPRESENTATION OF SET
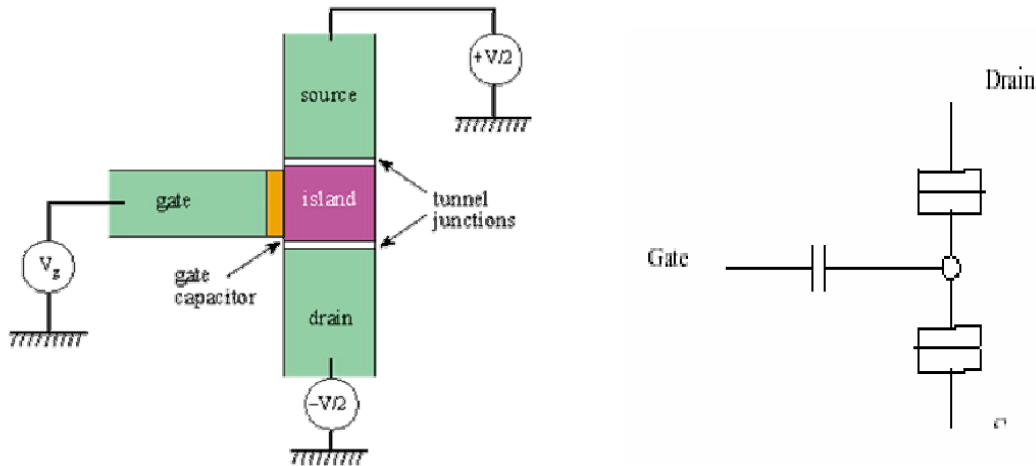
SIMPLIFIED STRUCTURE OF MOSFET

SINGLE ELECTRONIC TRANSISTOR SET

The structure of the typical SET consists of an isolated conductive island (single electron box) that is separated from the two external electrodes (source and drain) by tunneling junctions. The transfer of individual electrons between the electrodes and the Isolated island can be controlled by the voltage that is applied to the gate electrode, based on the fundamental principle of Coulomb blockade. The dimensions of the conductive island and the tunneling junctions need to be in the order of a few nanometers to a few tens of nanometers. While larger device dimensions allow observable device operation at very low temperatures, the dimensions may need to be reduced to sub-nanometer levels in order to achieve Coulomb blockade near room temperature.

Indeed, the device is reminiscent of a typicall MOSFET, but with a small conducting island embedded between two tunnel barriers, instead of the usual inversion channel. The current-voltage characteristics of the SET are as a function of different gate voltage levels. At small drain-to source voltage, there is no current since the tunneling rate is between the electrodes and the island is very low. This suppression of DC current at low voltage levels is known as the Coulomb blockade. At a certain threshold voltage, the Coulomb blockade is overcome, and for higher drain-to-source voltages, the current approaches one of its linear asymptotes.

The most important property of the single electron transistor is that the threshold voltage as well as the drain-to-source current in its vicinity is periodic functions of the gate voltage. The physical reason for these periodic functions of the gate voltage. The physical reason for this periodicity is the fact that the conditions that govern the tunneling

of charge between the electrodes and the isolated island can be established for consecutive, discrete states that correspond to the existence of integer multiples of an electron charge on the island. Still, it is evident that the device can be Operated as a switch controlled by the gate electrode, capable of performing a number of tasks. While the operation principles of the single electron transistor are dramatically different from those of classical MOS devices, the SET can also be seen, in very simple terms, as the limit case of MOSFET scaling where the traditional device behavior based on continuous charge flow in the conducting channel is replaced by discrete electron tunneling to the conducting island (electron box). In fact, one can conceivable think of few-electron (or several-electron) operation-as opposed to pure single-electron operation-as opposed to pure single-electron operation-to bridge the gap between classical MOSFETS and SETS. In any case, the novel properties of single-electron (or few-electron) devices appear to be offering some interesting and unconventional possibilities that can be exploited for the realization of switching functions.

DESIGN ASPECTS OF A SET CIRCUITS OR SYSTEMS:
ACCURACY AND RELIABILITY:
The yield, the reliability and the accuracy of the basic building blocks (SETS) arc expected to be inherently low due to fundamental limitations such as background charge effects. The low-level Circuit architectures as well as high-level system architectures consisting of SET elements must incorporate a very high degree of redundancy, fault-immunity, fault-tolerance, self-diagnosis, and self-repair properties to cope with in accuracy and reliability problems.
EXPLOTING SET CHARACTERISTICS:
SET devices exhibit particular characteristics, which are quite distinct from classical MOSFETS in terms of device behavior. In certain cases, it may be beneficial to exploit these operational characteristics in order to implement novel circuit functions.
### LOW LEVEL STRUCTURAL REGULARITY:
To ensure a simple fabrication process, high device density, better control of parasitic effects and better yield, it may be preferable to build *regular arrays* of SETS rather than irregularly arranged devices and interconnects. This constraint may be relaxed later when the fabrication processes reach maturity.

INTERCONNECT ISSUES:
Long distance interconnections between individual SET devices should be avoided. The interconnect problem is already becoming a dominant limitations for performance in conventional deep submicron CMOS technologies, and it is expected that the limitation would be much more severe for SET devices and technologies.

FAULT TOLERANT ARCHITECTURE FORSET:

LU=Logic unit
(AND /O R/N AND/N O T/MUX/D EMUX/ADD ER/
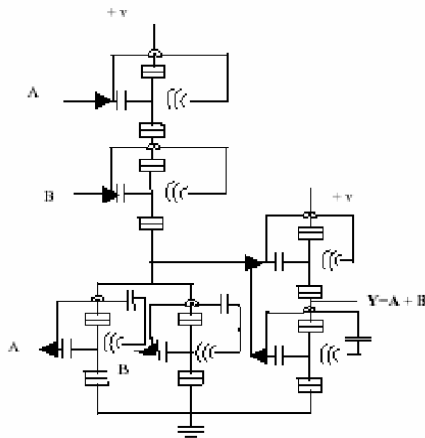S UB TRACTO R)
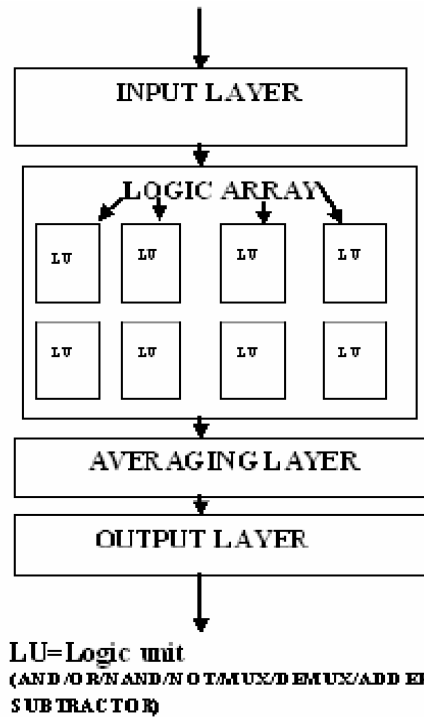
The proposed fault-tolerant architecture consists of four layers in which the data is strictly processed in a feed-forward manner. The first layer is denoted as the input layer, accepting conventional Boolean (binary) signal levels. The core operation is performed in the second layer, which consists of a number of identical, redundant units implementing the desired logic function. It will be seen that the fault immunity increases with the number of redundant units, yet the operation is quite different from the classical majority-based redundancy. The third layer receives the outputs of the redundant logic units in the second layer, creating a weighted average with rescaling. Note that the output of the third layer becomes a multiple-valued logic level. Finally, the fourth layer is the decision layer where a binary output value is extracted using a simple threshold function.

The typical weighted-averaging and rescaling function that is performed by one of the third-layer blocks. It was already shown in the literature that this particular type of weighted-sum functions can be implemented quite easily with SET devices our approach, the multiple-valued logic levels are not used to increase the information content of a signal, rather, they serve as a mechanism that allows reducing the impact of random device failures on the global transfer function surface. Hence, the multiple valued logic representation of the function provides an effective means for absorbing faults that would otherwise manifest themselves as catastrophic errors. In the simplest possible implementation, a single averaging block with equal weights already provides significant fault immunity. The benefits of this circuit architecture can be further increased by using multiple averaging units and/or different input weighting schemes. Since the averaging threshold unit is essentially shared by many logic units in the second layer, it can be designed using larger-geometry CMOS devices. This would reduce the vulnerability of the averaging function with respect to random failures and ensure sufficient output drive capability for the unit.
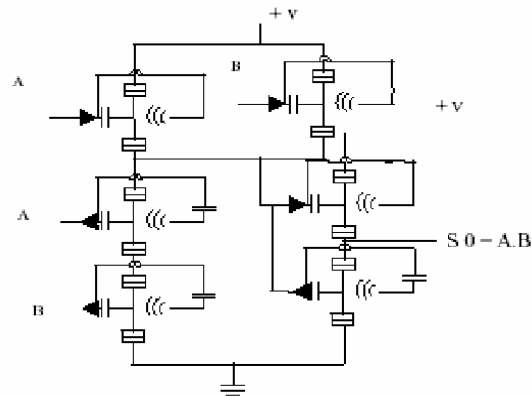
LOGIC CIRCUITS IMPLEMENTATION USING SET:

- **OR and AND:**

The following shown in the fig is Structure of 2-input OR Cell built with two identical logic units using SET. Here the input signal is A and B. Y is the output signal. Y=A+B. The NOR Realization of OR gate is employed here. Then another fig is Structure of 2-input AND Cell built with two identical logic units using SET. Here the input signal is X 1 and X2.The output signal is S0=A .B


OR Gate Implementation of SET: AND Gate Implementation of SET:

- **HALF ADDER and HALF SUBTRACTOR:**

The Half Adder was designed to add 2 - bit input A and B, The Outputs will be Sum and Carry signals named as S and C respectively. The output C=1, when A=1 and B=1. The output S=1, when A=1 or B=1. The Half Sub tractor was designed to add 2 - bit input a and b, The Outputs will be Difference and Borrow signals named   as D AND B repectively.The output
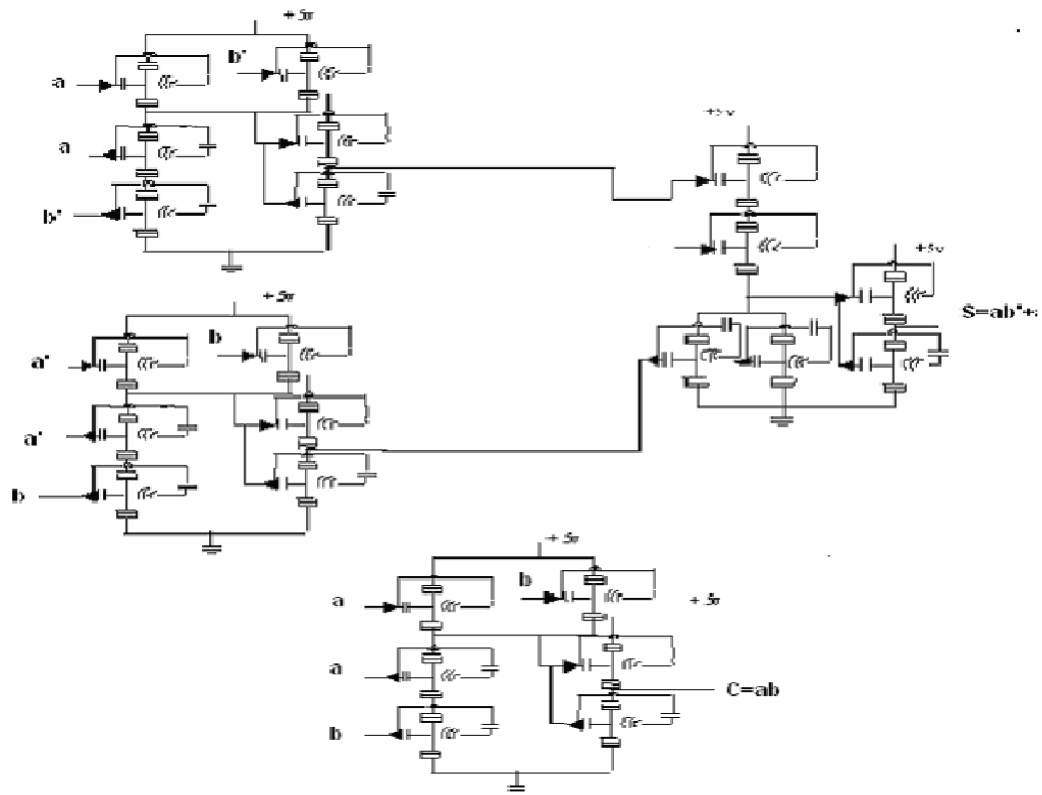
B=1, when a=0 and b=1. The output D=1, when A.B.

DEMERITS OF SET:

- Very high integration density and extremely low power dissipation
- Inherent sensitivity
- Background charge effects